i6

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR		ATTORNEY DOCKET NO.
08/937,877	09/29/97	TSYRGANOVICH	A	ZILG-183US0

EXAMINER	
SRIVASTAVA, V	
ART UNIT	**PAPER NUMBER**
2611	6

DATE MAILED: 06/05/01

TM01/0605

GERALD P PARSONS
MAJESTIC PARSONS SIEBERT AND HSUE
FOUR EMBARCADERO CENTER SUITE 1100
SAN FRANCISCO CA 94111-4106

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

Office Action Summary

Application No.	Applicant
08/937,877	Anatoliy V. Tsyrganovich
Examiner	**Art Unit**
Vivek Srivastava	2611

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) ☒ Responsive to communication(s) filed on *Dec 19, 2000*.

2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.

3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

Disposition of Claims

4) ☒ Claim(s) *1-31* is/are pending in the application.

4a) Of the above, claim(s) _____ is/are withdrawn from consideration.

5) ☒ Claim(s) *4, 5, 10, 12, and 31* is/are allowed.

6) ☒ Claim(s) *1-3, 6-9, 11, 13-20, 25, and 27-30* is/are rejected.

7) ☒ Claim(s) *21-24 and 26* is/are objected to.

8) ☐ Claims _____ are subject to restriction and/or election requirement.

Application Papers

9) ☐ The specification is objected to by the Examiner.

10) ☐ The drawing(s) filed on _____ is/are objected to by the Examiner.

11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved.

12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

13) ☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).

a) ☐ All b) ☐ Some* c) ☐ None of:

1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

*See the attached detailed Office action for a list of the certified copies not received.

14) ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

Attachment(s)

15) ☐ Notice of References Cited (PTO-892)
16) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
17) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s). _____
18) ☐ Interview Summary (PTO-413) Paper No(s). _____
19) ☐ Notice of Informal Patent Application (PTO-152)
20) ☐ Other:

DETAILED ACTION

Claim Rejections - 35 U.S.C. § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless --
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1 - 3, 6, 8, 9, 11, 13, 14 - 19, 25, 27 and 28 are rejected under 35 U.S.C. 102(b) as being anticipated by Kobayashi et al.

Considering claim 1, Kobayashi discloses a first circuit portion with a delay element (fig 5 item 22), a second circuit portion coupled to the first circuit portion including a delayed input (fig 5 item 26), an adjustment input not passing through the delay element (fig 5 item 27), wherein with no adjustment input the circuit acts as a filter (fig 5, when no adjusting is required and K1 and K2 equal to one, the circuit acts like a filter), wherein an adjustment input changes the level of the output (fig 5 adjustments coefficients K2 and K1 will change the level of output Dvec), wherein the second circuit portion adds the adjustment input to the at least one delayed signal input (figure 5, the signal K2 x Do(N+1) is added to the delayed or filtered signal K1 x DoN).

Considering claim 2, Kobayashi discloses the first circuit portion is a delay line (see fig 5 item 22).

Considering claim 3, Kobayashi discloses a second circuit which includes at lest one coefficient circuit connected to one of the at least one delayed signal inputs and to the adjustment input (see fig 5, second circuit, or coefficient circuit item 26 is connected to a delayed input and to adjustment input).

Considering claim 6, Kobayashi discloses a summer circuit to add the outputs of the coefficient circuit (fig 5 items 25 and 26, the circuit in claim 3/1 is assumed since applicant does not claim the second circuit).

Considering claim 8, Kobayashi discloses a differential phase input (see fig 5, differential phase input Do(N+1) is input to delay circuit).

Considering claim 9, Kobayashi inherently discloses the adjustment control logic adapted to provide the adjustment input (fig 5, col 4 lines 23 - 68).

Considering claim 11, Kobayashi discloses a second circuit portion which acts as a filter to the first input when there is not adjustment input (see fig 5, when no adjustment input is provided to circuit 26, the circuit functions as a filter).

Considering claim 13, Kobayashi discloses the claimed providing a circuit, inputting an input signal into the circuit such that the circuit filters the input signal to provide a filtered component to the output of the circuit (fig 5 items 21 and 22), inputting an adjustment signal into the circuit so that the adjustment signal provides an unfiltered offset to the output (fig 5

adjustments coefficients K2 and K1 will change the level of output Dvec), adding the adjustment signal to the input signal (figure 5, the signal K2 x Do(N+1) is added to the delayed or filtered signal K1 x DoN).

Considering claim 14, Kobayashi inherently discloses wherein the adjustment signal keeps the output within a preset range (col 4 lines 23 - 68, adjustment signal must keep output in a preset range in order to maintain a correct output).

Considering claims 15 and 19, Kobayashi discloses filtering of the input signal is a low-pass filtering (see frequency response in fig 6C from time t0 - t).

Considering claim 16, Kobayashi discloses the claimed wherein the input is a phase signal (col 4 lines 24 - 59).

Considering claims 17 and 27, Kobayashi discloses wherein the input is a hue signal (col 1 lines 7 - 11).

Considering claims 18 and 28, Kobayashi inherently discloses constraining a phase signal within a preset range (in order to adjust correct the phase, the output phase must be inherently constrained within a preset range) , the constraining step including adding a correction signal to the phase signal (fig 5), filtering the phase signal without filtering the correction signal portion of the phase signal (fig 5, when no adjusting is required, resulting in K2 and K1 equal to one, the circuits acts like a filter), and adding the correction signal to the phase signal (figure 5, the signal K2 x Do(N+1) is added to the delayed or filtered signal K1 x DoN).

Considering claim 25, Kobayashi discloses wherein the constraining step is such that the phase signal is processed so as to use a differential input (see fig 5, differential phase input Do(N+1) is input to delay circuit).

Claim Rejections - 35 U.S.C. § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 7, 20, 29 and 30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kobayashi et al in view of Namiki et al.

Considering claim 7, Kobayashi discloses wherein the first input and output are phase representations but fails to disclose an adjustment input causes an integer multiple of 180 deg (2pi) shift in the output signal.

Kobayashi discloses adjusting and converting the phase of a signal. Namiki teaches by shifting the phase by 180 deg (2pi) color distortion in a displayed television signal can be prevented. Therefore, it would have been obvious to one having ordinary skill in the art at the

time the invention was made to include shifting the phase by 180 deg or (2pi) to prevent color distortion in the displayed video signal.

Considering claim 20, Kobayashi fails to disclose wherein the correction signal is an integer multiple of 2pi.

Kobayashi discloses adjusting and converting the phase of a signal. Namiki teaches by shifting the phase by 180 deg (2pi) color distortion in a displayed television signal can be prevented. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to include shifting the phase by 180 deg or (2pi) to prevent color distortion in the displayed video signal.

Considering claim 29, Kobayashi discloses providing picture data including hue information encoded as phase having a first range (col 1 lines 5 - 11, col 4 lines 24 - 68, phase includes hue data encoded in a first phase range) and producing a filtered hue information signal with unfiltered offsets (fig 5, when no adjusting is required, K2 and K1 offsets are not filtered). Hue fails to disclose offsets of plus or minus 2pi.

Kobayashi discloses adjusting and correcting the phase of a signal. Namiki teaches by shifting the phase by 180 deg (2pi) color distortion in a displayed television signal can be prevented. It would have been obvious shifting the phase plus or minus 2pi, or shifting the phase 180 deg would have provide phase correction thus preventing color distortion. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made

to include shifting the phase by plus or minus 180 deg or (2pi) to prevent color distortion in the displayed video signal.

Considering claim 30, Kobayashi discloses producing a filtered hue information signal (fig 5, signal K1 x DoN is a filtered hue info signal) and adding the unfiltered offsets to the hue information signal (figure 5, the signal K2 x Do(N+1) is added to the delayed or filtered signal K1 x DoN).

Allowable Subject Matter

5. Claims 21 - 24 and 26 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

6. Claims 4, 5, 10, 12 and 31 are allowed.

7. The following is a statement of reasons for the indication of allowable subject matter: the prior art does not teach a circuit comprising a digital filter, coefficient multiplier circuitry adapted to multiply the signal values by filter coefficients, and a summer connected to the coefficient multiplier circuitry to produce and output value wherein the summing circuitry is connected to the

input lines of the signal values at different time indexes and to an adjustment input and the output of the summing circuitry is sent to a coefficient multiplying circuitry.

Response to Arguments

The Examiner agrees with Applicant's assertion that in figure 5 of Kobayashi, the input signal is multiplied by coefficients. However, as depicted in figure 5, the signal K2 x Do(N+1) is **added** to the delayed or filtered signal K1 x DoN. Claims 1, 13, 18 and 28 broadly recite adding a correction signal to a filtered input. This is clearly done in Kobayashi. As a result, the applicant's arguments are not persuasive.

Regarding Applicant's arguments to claims 7 and 20, the Applicant's openly admit that Namiki discloses shifting the phase by 180 deg. Although Namiki also discloses shifting by 0, 90, and 270, shifting the phase by 180 deg to prevent color distortion is not a novel feature and is not patentable. Namiki was introduced to teach phase distortion can be corrected by shifting the phase by 180 deg. Since Namiki discloses the claimed limitation the Applicant's arguments regarding claims 7 and 20 are not persuasive.

Regarding claim 29, in response to applicant's arguments against the references individually, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986).

Conclusion

8. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Isono et al (4,197,556) - Hue correction circuit

Sanada et al (4,091,411) - Color hue control circuit

Nakagawa et al (4,644,389) - Digital television signal processing circuit

Ekstrand (3,688,021) - Tint control

Yoshinaka et al (4,714,954) - Read start pulse generator for time base corrector

Kosaka et al (4,939,572) - Video signal processing apparatus

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks

Washington, D.C. 20231

or faxed to:

(703) 308-9051, (for formal communications intended for entry)

Or:

(703) 308- 5399 (for informal or draft communications, please label "PROPOSED" or "DRAFT")

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington. VA., Sixth Floor (Receptionist).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Vivek Srivastava whose telephone number is (703) 305 - 4038. The examiner can normally be reached on Monday - Thursday from 8:00 am to 5:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Andy Faile, can be reached at (703) 305 - 4380.

Any inquiry of a general nature or relating to the status of this application or proceeding

should be directed to the group receptionist whose telephone number is (703) 305 - 3900.

VS 5/29/01

ANDREW FAILE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600